NAVSTAR Simulator for Space-born Receivers

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Outline

• Global Positioning System
• Project motivation
• Project modules
• Project design parameters
• Project current status
• Conclusion
Global Positioning System

GPS satellites (NAVSTAR) → Channel → GPS receiver

Position
Velocity
Time

NAVSTAR Simulator Project
Project motivation

- This simulator will participate in testing of currently developing and other coming satellites.
- This project is one of the up-coming developing projects of the Egyptian Space Program (ESP).
- Prototype phase:
  - Graduation project
Simulator structure

- GPS Data frames generators
- GPS L/A code generator
- XOR
- IF
- Receiver power level calculator
- Doppler calculator
- GPS Satellites orbit propagator (position, velocity)
- Range determination
- GPS receiver location determination (position, velocity)
- One NAVSTAR satellite
- Noise generator
- Summing circuit
- DAC
- Mixer
- BPF
- LO
- RF Section
- PC program

GPS signal

~120dB
Project modules

- FPGA modules:
  - FPGA used is Vertex II Pro
  - C/A code and GPS frames generation
  - Modulator at intermediate frequency (IF)
  - Digital frequency synthesizer (frequency network)
  - The program uses the embedded micro-processors
  - Implementation using PowerPC® and MicroPlaze™
  - Orbit propagators
  - Antenna modeling
  - Doppler frequency calculator
  - Signal level calculator
  - Noise generator
Project modules

Three high current power supplies with continuous monitoring

Platform Flash for storing FPGA configurations

USB2 port for FPGA configurations

Compact flash card port for FPGA config and removable storage

PS/2 mouse and keyboard port

RS-232 serial port

High-speed expansion connector compatible with Digilent boards

Buttons, switches, and LEDs

Low-speed expansion connector compatible with Digilent boards

Virtex-II Pro XC2VP30 FPGA

SystemACE chips for Compact Flash I/O

SATA connectors for Gigabit serial I/O

10/100 Ethernet MAC/PHY

Stereo audio via AC97 codec

Power connector and switch

XSGA Video Port

SDRAM DIMM slot holds up to 2GBytes

6/16/2010
Project modules

• PC program
  o Initial data to simulator
  o Registration of receiver’s data
  o Simulator assessment (post session assessment)

• Digital-to-Analog converter (DAC)
  o Convert the simulator IF signal from its digital form to its analog equivalent form

• RF section
  o Generates the GPS transmitter RF signal at L1 frequency
## Design parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Frequency</td>
<td>L1: 1575.42 MHz</td>
</tr>
<tr>
<td>Number of simulated satellites</td>
<td>32</td>
</tr>
<tr>
<td>Number of simulated channels</td>
<td>12 (max)</td>
</tr>
<tr>
<td>Channels Type</td>
<td>GPS C/A code</td>
</tr>
<tr>
<td>Max Velocity (velocity of GPS receiver in orbit)</td>
<td>Up to 10 km/s</td>
</tr>
<tr>
<td>Pseudorange accuracy</td>
<td>5 m</td>
</tr>
<tr>
<td>Pseudorange Rate accuracy</td>
<td>1 m/s</td>
</tr>
<tr>
<td>Delta Pseudorange accuracy</td>
<td>1 m</td>
</tr>
<tr>
<td>Inter-channel Bias</td>
<td>0</td>
</tr>
<tr>
<td>Signal level</td>
<td>-145 dBm ± 15 dB</td>
</tr>
<tr>
<td>Number of RF Outputs</td>
<td>1</td>
</tr>
<tr>
<td>User interfaces</td>
<td></td>
</tr>
<tr>
<td>Control interface</td>
<td>RS232</td>
</tr>
<tr>
<td>RF output</td>
<td>SMA</td>
</tr>
</tbody>
</table>

96/16/2010
Current status

• Prototype phase
  o Graduation project, i.e. sticking to academic year schedule
  o 70% of work is done
  o integration and Testing of main blocks is going on
Conclusion

- Manufacturing the prototype
- Testing and debugging the prototype
- Electromagnetic interference (EMI) testing
THANK YOU FOR YOUR ATTENTION